

What is claimed is

1           1.    A frame synchronization detecting circuit  
2 comprising:

3           a frame synchronization pattern detecting means for  
4 detecting, with specified timing, a predetermined frame  
5 synchronization pattern contained in received data having a frame  
6 structure;

7           a hunting state judging means for judging whether said frame  
8 synchronization detecting circuit is in a hunting state in which  
9 said predetermined frame synchronization pattern is being sought,  
10 based on a detection result obtained by said frame synchronization  
11 pattern detecting means; and

12          a timing stopping means for stopping said timing of detecting  
13 said predetermined frame synchronization pattern only for a  
14 specified period of time before and after a frame pulse is generated  
15 which indicates a head of a frame containing said received data  
16 when said frame synchronization detecting circuit is judged to  
17 be in said hunting state by said hunting state judging means.

1           2.    The frame synchronization detecting circuit  
2 according to Claim 1, further comprising a resetting means for  
3 resetting frame synchronization detecting operations to be  
4 performed by said frame synchronization pattern detecting means  
5 and said hunting state judging means at a time other than said  
6 specified period of time before and after said frame pulse is  
7 generated when said frame synchronization detecting circuit is  
8 judged to be in said hunting state by said hunting state judging  
9 means.

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1           3.    The frame synchronization detecting circuit  
2   according to Claim 2, wherein said stopping by said timing stopping  
3   means and said resetting by said resetting means are performed  
4   with different timing.

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1           4.    A frame synchronization detecting circuit  
2   comprising:

3           a frame synchronization pattern detecting means for  
4   detecting a predetermined frame synchronization pattern contained  
5   in received data having a frame structure;

6           a hunting state judging means for judging whether said frame  
7   synchronization detecting circuit is in a hunting state in which  
8   said predetermined frame synchronization pattern is being sought,  
9   based on a detection result obtained by said frame synchronization  
10   pattern detecting means; and

11          a received data fixing means for making said received data  
12   fixed only for a specified period of time before and after a frame  
13   pulse is generated which indicates a head of a frame containing  
14   said received data when said frame synchronization detecting  
15   circuit is judged to be in said hunting state by said hunting state  
16   judging means.

1           5.    A frame synchronization detecting circuit  
2   comprising:

3           a frame synchronization pattern detecting means for  
4   detecting a predetermined frame synchronization pattern contained  
5   in received data having a frame structure;

6           a hunting state judging means for judging whether said frame  
7   synchronization detecting circuit is in a hunting state in which

8 said predetermined frame synchronization pattern is being sought,  
9 based on a detection result obtained by said frame synchronization  
10 pattern detecting means; and

11 a resetting means for resetting frame synchronization  
12 detecting operations to be performed by said frame synchronization  
13 pattern detecting means and said hunting state judging means at  
14 a time other than said specified period of time before and after  
15 said frame pulse is generated when said frame synchronization  
16 detecting circuit is judged to be in said hunting state by said  
17 hunting state judging means.

1 6. A frame synchronization detecting circuit  
2 comprising:

3 a frame synchronization pattern detecting means for  
4 detecting a predetermined frame synchronization pattern contained  
5 in received data having a frame structure;

6 a hunting state judging means for judging whether said frame  
7 synchronization detecting circuit is in a hunting state in which  
8 said predetermined frame synchronization pattern is being sought,  
9 based on a detection result obtained by said frame synchronization  
10 pattern detecting means; and

11 a circuit stop controlling means for stopping an operation  
12 of a circuit connected to a front stage only for a specified period  
13 of time before and after a frame pulse is generated when said frame  
14 synchronization detecting circuit is judged to be in said hunting  
15 state by said hunting state judging means.

1 7. The frame synchronization detecting circuit  
2 according to Claim 6, wherein said circuit stop controlling means,

3 when canceling a stop of operations of said circuit, cancels said  
4 stop of operations of said circuit connected to said front stage  
5 after it has canceled a stop of timing of frame synchronization  
6 detection operations.

8. A frame synchronization detecting circuit comprising:

10 a frame synchronization pattern detecting means for detecting a predetermined frame synchronization pattern contained in received data having a frame structure;

15 a hunting state judging means for judging whether said frame synchronization detecting circuit is in a hunting state in which said predetermined frame synchronization pattern is being sought, based on a detection result obtained by said frame synchronization pattern detecting means; and

20 a circuit operation stopping means for stopping operations of, at least, a part of said frame synchronization detecting circuit only for a specified period of time before and after a frame pulse is generated which indicates a head of a frame containing said received data when said frame synchronization detecting circuit is judged to be in said hunting state by said hunting state judging means.

1 9. A frame synchronization detecting circuit comprising:

3 a frame synchronization pattern detecting circuit for detecting, with specified timing, a predetermined frame synchronization pattern contained in received data having a frame  
5 structure;  
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7 a hunting state judging circuit for judging whether said  
8 frame synchronization detecting circuit is in a hunting state in  
9 which said predetermined frame synchronization pattern is being  
10 sought, based on a detection result obtained by said frame  
11 synchronization pattern detecting circuit; and

12 a timing stopping circuit for stopping said timing of  
13 detecting said predetermined frame synchronization pattern only  
14 for a specified period of time before and after a frame pulse is  
15 generated which indicates ahead of a frame containing said received  
16 data when said frame synchronization detecting circuit is judged  
17 to be in said hunting state by said hunting state judging circuit.

1 10. The frame synchronization detecting circuit  
2 according to Claim 9, further comprising a resetting circuit for  
3 resetting frame synchronization detecting operations to be  
4 performed by said frame synchronization pattern detecting circuit  
5 and said hunting state judging circuit at a time other than said  
6 specified period of time before and after said frame pulse is  
7 generated when said frame synchronization detecting circuit is  
8 judged to be in said hunting state by said hunting state judging  
9 circuit.

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1 11. The frame synchronization detecting circuit  
2 according to Claim 10, wherein said stopping by said timing stopping  
3 circuit and said resetting by said resetting circuit are performed  
4 with different timing.

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1 12. A frame synchronization detecting circuit  
2 comprising:

3 a frame synchronization pattern detecting circuit for  
4 detecting a predetermined frame synchronization pattern contained  
5 in received data having a frame structure;

6 a hunting state judging circuit for judging whether said  
7 frame synchronization detecting circuit is in a hunting state in  
8 which said predetermined frame synchronization pattern is being  
9 sought, based on a detection result obtained by said frame  
10 synchronization pattern detecting circuit; and

11 a received data fixing circuit for making said received data  
12 fixed only for a specified period of time before and after a frame  
13 pulse is generated which indicates a head of a frame containing  
14 said received data when said frame synchronization detecting  
15 circuit is judged to be in said hunting state by said hunting state  
16 judging circuit.

1 13. A frame synchronization detecting circuit  
2 comprising:

3 a frame synchronization pattern detecting circuit for  
4 detecting a predetermined frame synchronization pattern contained  
5 in received data having a frame structure;

6 a hunting state judging circuit for judging whether said  
7 frame synchronization detecting circuit is in a hunting state in  
8 which said predetermined frame synchronization pattern is being  
9 sought, based on a detection result obtained by said frame  
10 synchronization pattern detecting circuit; and

11 a resetting circuit for resetting frame synchronization  
12 detecting operations to be performed by said frame synchronization  
13 pattern detecting circuit and said hunting state judging circuit  
14 at a time other than said specified period of time before and after

15 said frame pulse is generated when said frame synchronization  
16 detecting circuit is judged to be in said hunting state by said  
17 hunting state judging circuit.

1 14. A frame synchronization detecting circuit  
2 comprising:

3 a frame synchronization pattern detecting circuit for  
4 detecting a predetermined frame synchronization pattern contained  
5 in received data having a frame structure;

6 a hunting state judging circuit for judging whether said  
7 frame synchronization detecting circuit is in a hunting state in  
8 which said predetermined frame synchronization pattern is being  
9 sought, based on a detection result obtained by said frame  
10 synchronization pattern detecting circuit; and

11 a stop controlling circuit for stopping an operation of a  
12 circuit connected to a front stage only for a specified period  
13 of time before and after a frame pulse is generated when said frame  
14 synchronization detecting circuit is judged to be in said hunting  
15 state by said hunting state judging circuit.

1 15. The frame synchronization detecting circuit  
2 according to Claim 14, wherein said stop controlling circuit, when  
3 canceling a stop of operations of said circuit, cancels said stop  
4 of operations of said circuit connected to said front stage after  
5 it has canceled a stop of timing of frame synchronization detection  
6 operations.

1 16. A frame synchronization detecting circuit  
2 comprising:

3           a frame synchronization pattern detecting circuit for  
4     detecting a predetermined frame synchronization pattern contained  
5     in received data having a frame structure;

6           a hunting state judging circuit for judging whether said  
7     frame synchronization detecting circuit is in a hunting state in  
8     which said predetermined frame synchronization pattern is being  
9     sought, based on a detection result obtained by said frame  
10    synchronization pattern detecting circuit; and

11          an operation stopping circuit for stopping operations of,  
12    at least, a part of said frame synchronization detecting circuit  
13    only for a specified period of time before and after a frame pulse  
14    is generated which indicates a head of a frame containing said  
15    received data when said frame synchronization detecting circuit  
16    is judged to be in said hunting state by said hunting state judging  
17    circuit.